

DATA SHEET

74ALVCH32501

36-bit universal bus transceiver with
direction pin; 3-state

Product specification
Supersedes data of 2000 Mar 16

2004 Oct 13

36-bit universal bus transceiver with direction pin; 3-state

74ALVCH32501

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- Current drive ± 24 mA at 3.0 V
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparent, latched or clocked mode
- CMOS low power consumption
- Direct interface with TTL levels
- All inputs have bus-hold circuitry
- Output drive capability 50 Ω transmission lines at 85 °C
- Plastic fine-pitch ball grid array package.

DESCRIPTION

The 74ALVCH32501 is a high-performance CMOS product designed for V_{CC} operation at 2.5 V and 3.3 V.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The 74ALVCH32501 can be used as two 18-bit transceivers or one 36-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OE_{AB} and $\overline{OE}_{BA}$), latch enable (LE_{AB} and LE_{BA}), and clock inputs (CP_{AB} and CP_{BA}). For A-to-B data flow, the device operates in the transparent mode when LE_{AB} is HIGH. When input LE_{AB} is LOW, the A data is latched if input CP_{AB} is held at a HIGH or LOW level. If input LE_{AB} is LOW, the A data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CP_{AB} . When input OE_{AB} is HIGH, the outputs are active. When input OE_{AB} is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B, but uses inputs $\overline{OE}_{BA}$, LE_{BA} and CP_{BA} . The output enables are complementary (OE_{AB} is active HIGH, and $\overline{OE}_{BA}$ is active LOW).

To ensure the high-impedance state during power-up or power-down, pin $\overline{OE}_{BA}$ should be tied to V_{CC} through a pull-up resistor and pin OE_{AB} should be tied to GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sinking or current-sourcing capability of the driver.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n ; B_n to A_n	$C_L = 30$ pF; $V_{CC} = 2.5$ V	2.8	ns
		$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.0	ns
C_I	input capacitance		4.0	pF
$C_{I/O}$	input/output capacitance		8.0	pF
C_{PD}	power dissipation capacitance per latch	$V_I = GND$ to V_{CC} ; note 1		
		outputs enabled	21	pF
		outputs disabled	3	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

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FUNCTION TABLE

See notes 1 and 2.

INPUT				INTERNAL REGISTERS	OUTPUT	OPERATING MODE
nOE _{AB}	nLE _{AB}	nCP _{AB}	nA _n		nB _n	
L	H	X	X	X	Z	disabled
L	↓	X	h	H	Z	disabled; latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	disabled; hold data
L	L	↑	h	H	Z	disabled; clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	latch data and display
H	↓	X	l	L	L	
H	L	↑	h	H	H	clock data and display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	hold data and display
H	L	H or L	X	L	L	

Notes

1. A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{nOE}_{BA}$, nLE_{BA} and nCP_{BA} .
2. H = HIGH voltage level;
h = HIGH voltage level on set-up time prior to the enable or clock transition;
L = LOW voltage level;
l = LOW voltage level on set-up time prior to the enable or clock transition;
NC = no change;
X = don't care;
↑ = LOW-to-HIGH enable or clock transition;
↓ = HIGH-to-LOW enable or clock transition;
Z = high impedance OFF-state.

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74ALVCH32501EC	−40 °C to +85 °C	114	LFBGA114	plastic	SOT537-1

PINNING

SYMBOL	DESCRIPTION
nA _n	data inputs
nB _n	data outputs
GND	ground (0 V)
V _{CC}	DC supply voltage
nOE _{AB}	output enable inputs A to B (active HIGH)
n $\overline{\text{OE}}$ _{BA}	output enable inputs B to A (active LOW)
nLE _{AB}	latch enable inputs A to B
nLE _{BA}	latch enable inputs B to A
nCP _{AB}	clock input A to B
nCP _{BA}	clock input B to A

6	1B ₁	1B ₃	1B ₅	1B ₇	1B ₉	1B ₁₁	1B ₁₃	1B ₁₄	1B ₁₆	n.c.	2B ₁	2B ₃	2B ₅	2B ₇	2B ₉	2B ₁₁	2B ₁₃	2B ₁₄	2B ₁₆
5	1B ₀	1B ₂	1B ₄	1B ₆	1B ₈	1B ₁₀	1B ₁₂	1B ₁₅	1B ₁₇	2CP _{AB}	2B ₀	2B ₂	2B ₄	2B ₆	2B ₈	2B ₁₀	2B ₁₂	2B ₁₅	2B ₁₇
4	1CP _{AB}	GND	GND	V _{CC}	GND	GND	V _{CC}	GND	1CP _{BA}	GND	GND	GND	V _{CC}	GND	GND	V _{CC}	GND	2CP _{BA}	GND
3	1LE _{AB}	1OE _{AB}	GND	V _{CC}	GND	GND	V _{CC}	GND	1 $\overline{\text{OE}}$ _{BA}	1LE _{BA}	2OE _{AB}	GND	V _{CC}	GND	GND	V _{CC}	GND	2 $\overline{\text{OE}}$ _{BA}	2LE _{BA}
2	1A ₀	1A ₂	1A ₄	1A ₆	1A ₈	1A ₁₀	1A ₁₂	1A ₁₅	1A ₁₇	2LE _{AB}	2A ₀	2A ₂	2A ₄	2A ₆	2A ₈	2A ₁₀	2A ₁₂	2A ₁₅	2A ₁₇
1	1A ₁	1A ₃	1A ₅	1A ₇	1A ₉	1A ₁₁	1A ₁₃	1A ₁₄	1A ₁₆	n.c.	2A ₁	2A ₃	2A ₅	2A ₇	2A ₉	2A ₁₁	2A ₁₃	2A ₁₄	2A ₁₆
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

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Fig.1 Pin configuration.

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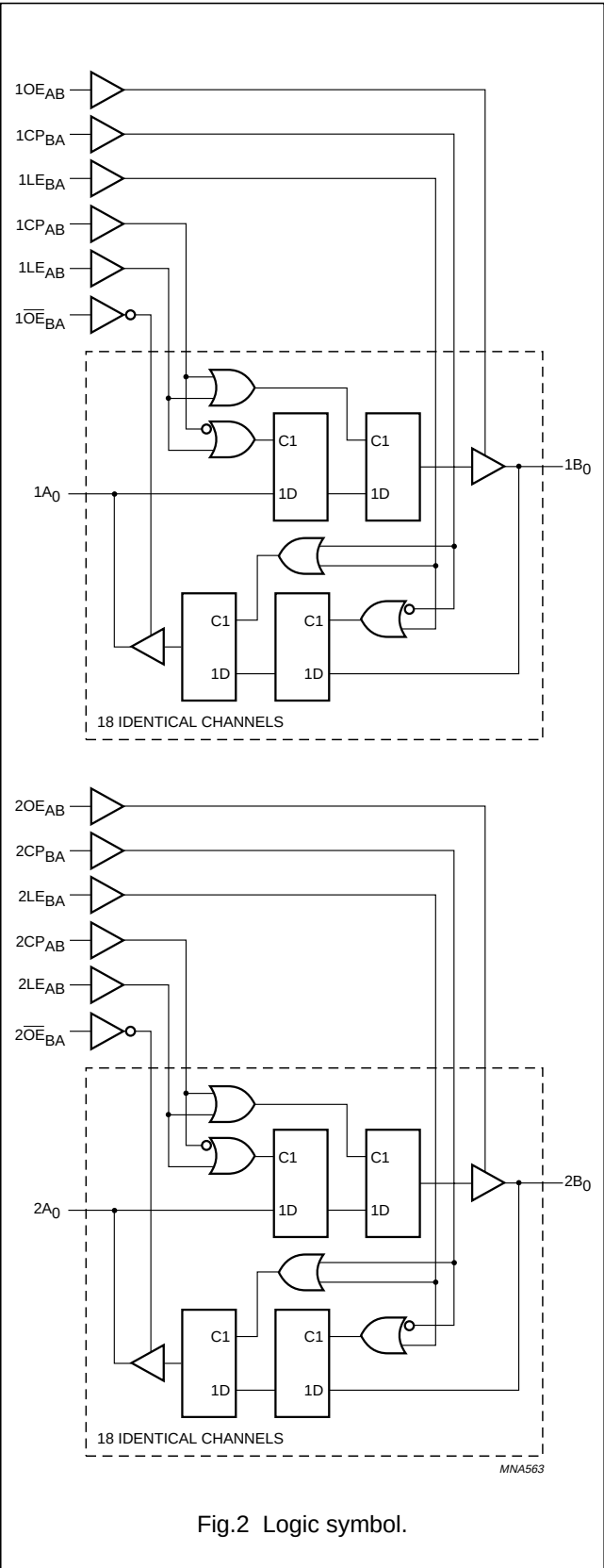


Fig.2 Logic symbol.

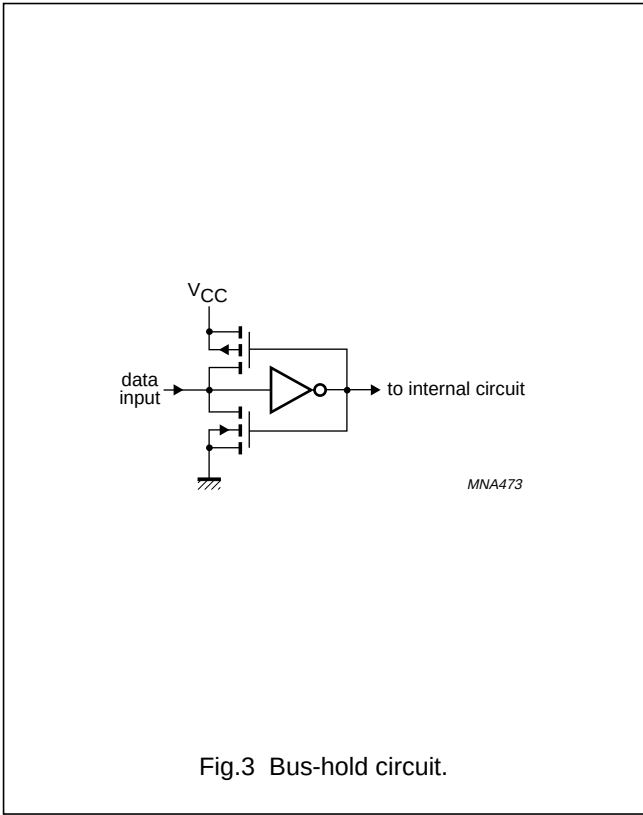


Fig.3 Bus-hold circuit.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage	2.5 V range (for maximum speed performance at 30 pF output load)	2.3	2.7	V
		3.3 V range (for maximum speed performance at 50 pF output load)	3.0	3.6	V
V _I	input voltage		0	V _{CC}	V
V _O	output voltage	output HIGH or LOW state	0	V _{CC}	V
T _{amb}	ambient temperature		−40	+85	°C
t _r , t _f	input rise and fall time ratios (Δt/ΔV)	V _{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		−0.5	+4.6	V
V _I	input voltage	for control pins; note 1	−0.5	+4.6	V
		for data input pins; note 1	−0.5	V _{CC} + 0.5	V
I _{IK}	input diode current	V _I < 0 V	−	−50	mA
I _{OK}	output clamping diode current	V _O < 0 V; note 1	−	50	mA
V _O	output voltage	see note 1	−0.5	V _{CC} + 0.5	V
I _O	output sink current	V _O = 0 V to V _{CC}	−	−50	mA
I _{CC} , I _{GND}	V _{CC} or GND current		−	±100	mA
T _{stg}	storage temperature		−65	+150	°C
P _{tot}	power dissipation	T _{amb} = −40 °C to +85 °C; note 2	−	1000	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P_{tot} derates linearly with 1.8 mW/K.

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DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = –40 °C to +85 °C							
V _{IH}	HIGH-level input voltage		2.3 to 2.7	1.7	1.2	–	V
			2.7 to 3.6	2.0	1.5	–	V
V _{IL}	LOW-level input voltage		2.3 to 2.7	–	1.2	0.7	V
			2.7 to 3.6	–	1.5	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –100 μA I _O = –6 mA I _O = –12 mA I _O = –12 mA I _O = –12 mA I _O = –24 mA	2.3 to 3.6	V _{CC} – 0.2	V _{CC}	–	V
			2.3	V _{CC} – 0.3	V _{CC} – 0.08	–	V
			2.3	V _{CC} – 0.6	V _{CC} – 0.26	–	V
			2.7	V _{CC} – 0.5	V _{CC} – 0.14	–	V
			3.0	V _{CC} – 0.6	V _{CC} – 0.09	–	V
			3.0	V _{CC} – 1.0	V _{CC} – 0.28	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA I _O = 6 mA I _O = 12 mA I _O = 12 mA I _O = 24 mA	2.3 to 3.6	–	GND	0.20	V
			2.3	–	0.07	0.40	V
			2.3	–	0.15	0.70	V
			2.7	–	0.14	0.40	V
			3.0	–	0.27	0.55	V
I _I	input leakage current	V _I = V _{CC} or GND	2.3 to 3.6	–	±0.1	±5	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; note 2	2.3 to 3.6	–	0.1	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	2.3 to 3.6	–	0.4	80	μA
ΔI _{CC}	additional quiescent supply current given per data I/O pin with bus-hold	V _I = V _{CC} – 0.6 V; I _O = 0 A	2.7 to 3.6	–	150	750	μA
I _{BHL}	bus-hold LOW sustaining current	V _I = 0.7 V; note 3	2.3	45	–	–	μA
		V _I = 0.8 V; note 3	3.0	75	150	–	μA
I _{BHH}	bus-hold HIGH sustaining current	V _I = 1.7 V; note 3	2.3	–45	–	–	μA
		V _I = 2.0 V; note 3	3.0	–75	–175	–	μA
I _{BHLO}	bus-hold LOW overdrive current	note 3	3.6	500	–	–	μA
I _{BHHO}	bus-hold HIGH overdrive current	note 3	3.6	–500	–	–	μA

Notes

1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For I/O ports, the parameter I_{OZ} includes the input leakage current.
3. Valid for data inputs of bus-hold parts.

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AC CHARACTERISTICS

 $T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}; \text{GND} = 0\text{ V}$

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L				
V _{CC} = 2.3 V to 2.7 V; t _r = t _f ≤ 2.0 ns; note 1							
t _{PHL} /t _{PLH}	propagation delay						
	nA _n to nB _n ; nB _n to nA _n	see Figs 4 and 8	30 pF	1.0	2.8	5.1	ns
	nLE _{BA} to nA _n ; nLE _{AB} to nB _n	see Figs 5 and 8	30 pF	1.1	3.5	6.1	ns
	nCP _{BA} to nA _n ; nCP _{AB} to nB _n	see Figs 5 and 8	30 pF	1.0	3.3	6.1	ns
t _{PZH} /t _{PZL}	3-state output enable time nOE _{AB} to nB _n	see Figs 6 and 8	30 pF	1.0	2.5	5.8	ns
	3-state output enable time nOE _{BA} to nA _n	see Figs 6 and 8	30 pF	1.3	2.8	6.3	ns
t _{PHZ} /t _{PLZ}	3-state output disable time nOE _{AB} to nB _n	see Figs 6 and 8	30 pF	1.5	2.5	6.2	ns
	3-state output disable time nOE _{BA} to nA _n	see Figs 6 and 8	30 pF	1.3	2.5	5.3	ns
t _W	nLE _{AB} or nLE _{BA} pulse width HIGH	see Figs 5 and 8	30 pF	3.3	0.8	–	ns
	nCP _{AB} or nCP _{BA} pulse width HIGH or LOW	see Figs 5 and 8	30 pF	3.3	2.0	–	ns
t _{su}	set-up time nA _n before nCP _{AB} ↑ or nB _n before nCP _{BA} ↑	see Figs 7 and 8	30 pF	1.7	0.1	–	ns
	set-up time CP HIGH or LOW nA _n before nLE _{AB} ↓ or nB _n before nLE _{BA} ↓	see Figs 7 and 8	30 pF	1.1	0.1	–	ns
t _h	hold time nA _n after nCP _{AB} ↑ or nB _n after nCP _{BA} ↑	see Figs 7 and 8	30 pF	1.7	0.3	–	ns
	hold time CP HIGH or LOW nA _n after nLE _{AB} ↓ or nB _n after nLE _{BA} ↓	see Figs 7 and 8	30 pF	1.6	0.3	–	ns
f _{max}	maximum clock frequency	see Figs 5 and 8	30 pF	150	330	–	MHz
V _{CC} = 2.7 V; t _r = t _f ≤ 2.5 ns; note 2							
t _{PHL} /t _{PLH}	propagation delay						
	nA _n to nB _n ; nB _n to nA _n	see Figs 4 and 8	50 pF	–	3.0	4.6	ns
	nLE _{BA} to nA _n ; nLE _{AB} to nB _n	see Figs 5 and 8	50 pF	–	3.6	5.3	ns
	nCP _{BA} to nA _n ; nCP _{AB} to nB _n	see Figs 5 and 8	50 pF	–	3.4	5.6	ns
t _{PZH} /t _{PZL}	3-state output enable time nOE _{AB} to nB _n	see Figs 6 and 8	50 pF	–	2.7	5.3	ns
	3-state output enable time nOE _{BA} to nA _n	see Figs 6 and 8	50 pF	–	3.3	6.0	ns
t _{PHZ} /t _{PLZ}	3-state output disable time nOE _{AB} to nB _n	see Figs 6 and 8	50 pF	–	3.6	5.7	ns
	3-state output disable time nOE _{BA} to nA _n	see Figs 6 and 8	50 pF	–	3.3	4.6	ns
t _W	pulse width nLE _{AB} or nLE _{BA} HIGH	see Figs 5 and 8	50 pF	3.3	0.7	–	ns
	pulse width nCP _{AB} or nCP _{BA} HIGH or LOW	see Figs 5 and 8	50 pF	3.3	1.4	–	ns
t _{su}	set-up time nA _n before nCP _{AB} ↑ or nB _n before nCP _{BA} ↑	see Figs 7 and 8	50 pF	+1.4	–0.1	–	ns
	set-up time CP HIGH or LOW nA _n before nLE _{AB} ↓ or nB _n before nLE _{BA} ↓	see Figs 7 and 8	50 pF	+1.0	–0.2	–	ns

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L				
t _h	hold time nA _n after nCP _{AB} ↑ or nB _n after nCP _{BA} ↑	see Figs 7 and 8	50 pF	1.6	0.3	–	ns
	hold time CP HIGH or LOW nA _n after nLE _{AB} ↓ or nB _n after nLE _{BA} ↓	see Figs 7 and 8	50 pF	1.5	0.1	–	ns
f _{max}	maximum clock frequency	see Figs 5 and 8	50 pF	150	333	–	MHz
V_{CC} = 3.0 V to 3.6 V; t_r = t_f ≤ 2.5 ns; note 3							
t _{PHL} /t _{PLH}	propagation delay nA _n to nB _n ; nB _n to nA _n	see Figs 4 and 8	50 pF	1.0	3.0	4.2	ns
	nLE _{BA} to nA _n ; nLE _{AB} to nB _n	see Figs 5 and 8	50 pF	1.3	3.4	4.8	ns
	nCP _{BA} to nA _n ; nCP _{AB} to nB _n	see Figs 5 and 8	50 pF	1.4	3.3	4.9	ns
t _{PZH} /t _{PZL}	3-state output enable time nOE _{AB} to nB _n	see Figs 6 and 8	50 pF	1.0	2.4	4.6	ns
	3-state output enable time nOE _{BA} to nA _n	see Figs 6 and 8	50 pF	1.1	2.5	5.0	ns
t _{PHZ} /t _{PLZ}	3-state output disable time nOE _{AB} to nB _n	see Figs 6 and 8	50 pF	1.4	2.9	5.0	ns
	3-state output disable time nOE _{BA} to nA _n	see Figs 6 and 8	50 pF	1.3	3.1	4.2	ns
t _w	pulse width nLE _{AB} or nLE _{BA} HIGH	see Figs 5 and 8	50 pF	3.3	0.9	–	ns
	pulse width nCP _{AB} or nCP _{BA} HIGH or LOW	see Figs 5 and 8	50 pF	3.3	1.1	–	ns
t _{su}	set-up time nA _n before nCP _{AB} ↑ or nB _n before nCP _{BA} ↑	see Figs 7 and 8	50 pF	+1.3	–0.3	–	ns
	set-up time CP HIGH or LOW nA _n before nLE _{AB} ↓ or nB _n before nLE _{BA} ↓	see Figs 7 and 8	50 pF	1.0	0.3	–	ns
t _h	hold time nA _n after nCP _{AB} ↑ or nB _n after nCP _{BA} ↑	see Figs 7 and 8	50 pF	+1.3	–0.4	–	ns
	hold time CP HIGH or LOW nA _n after nLE _{AB} ↓ or nB _n after nLE _{BA} ↓	see Figs 7 and 8	50 pF	1.2	0.1	–	ns
f _{max}	maximum clock frequency	see Figs 5 and 8	50 pF	150	340	–	MHz

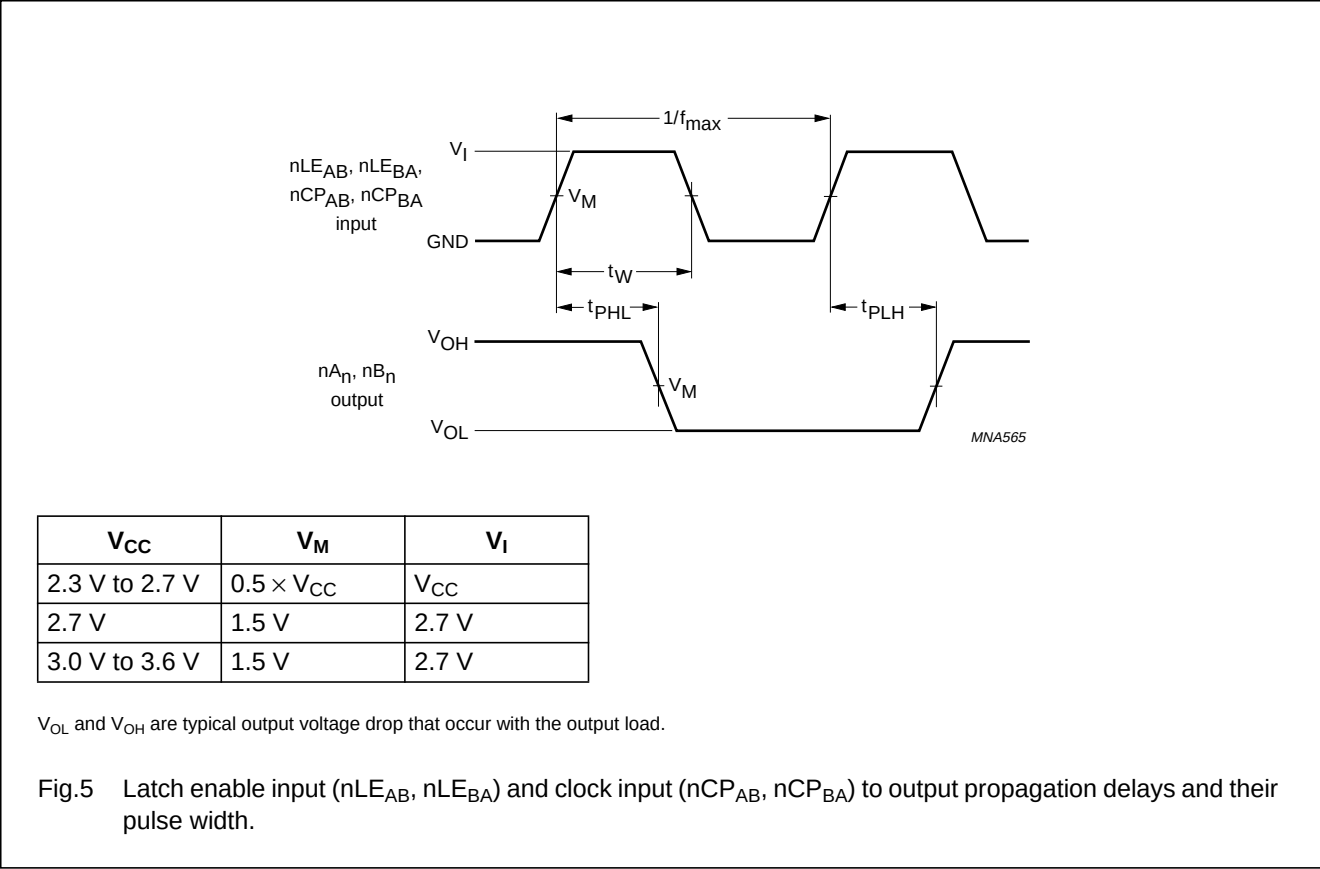
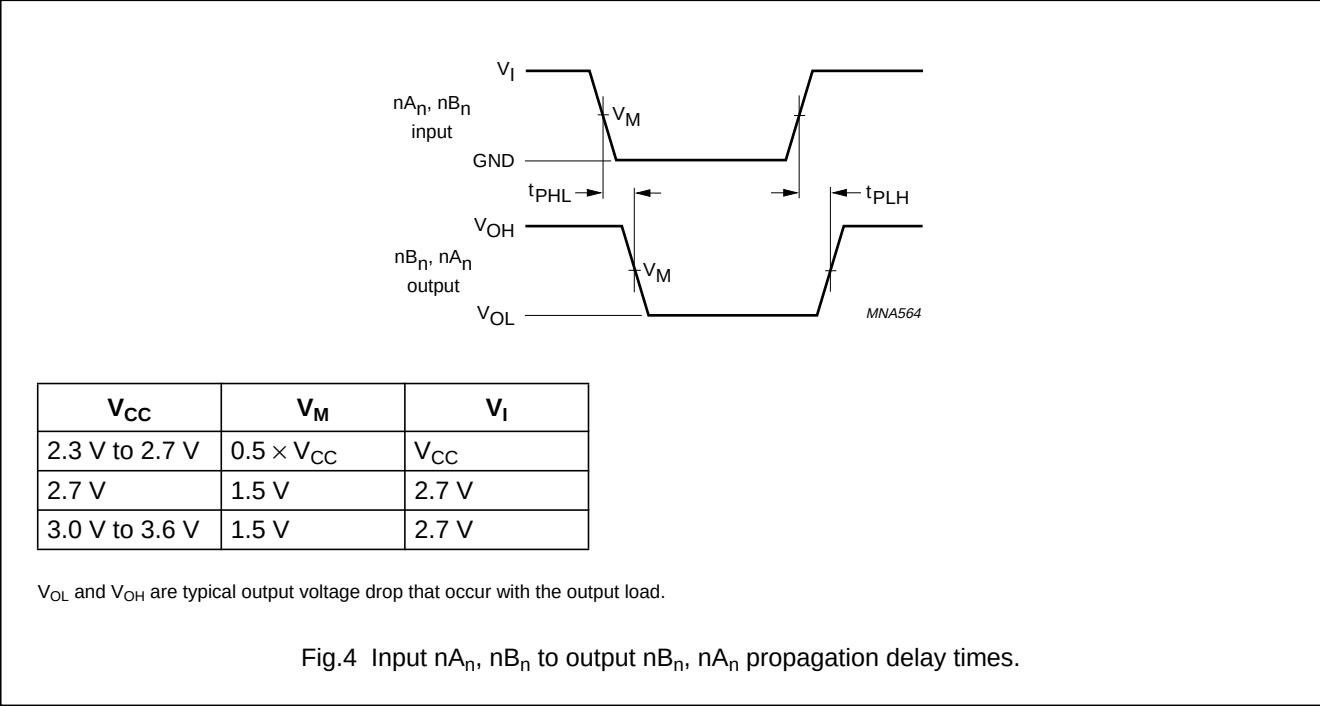
Notes

1. All typical values are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
2. All typical values are measured at T_{amb} = 25 °C.
3. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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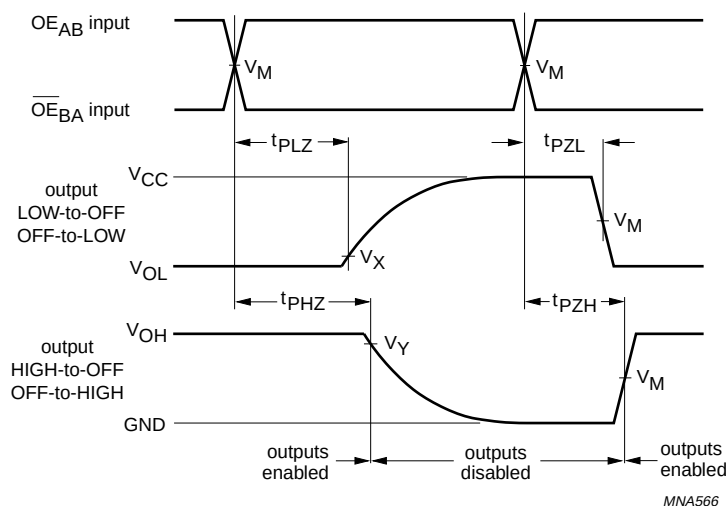
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AC WAVEFORMS



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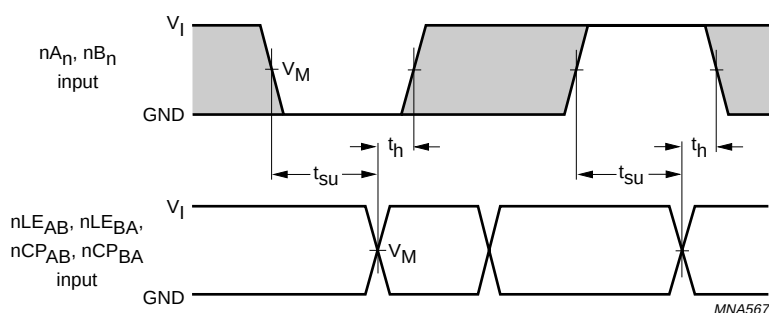
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V_{CC}	V_M	V_X	V_Y	V_I
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$V_{OL} + 150 \text{ mV}$	$V_{OH} - 150 \text{ mV}$	V_{CC}
2.7 V	1.5 V	$V_{OL} + 300 \text{ mV}$	$V_{OH} - 300 \text{ mV}$	2.7 V
3.0 V to 3.6 V	1.5 V	$V_{OL} + 300 \text{ mV}$	$V_{OH} - 300 \text{ mV}$	2.7 V

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

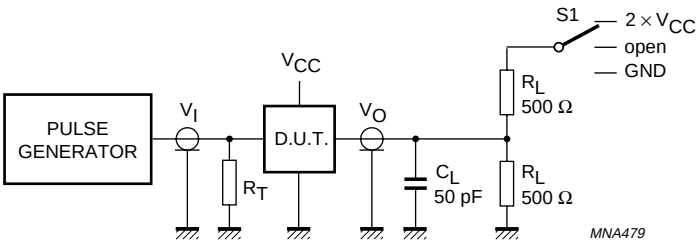
V_{CC}	V_M	V_I
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}
2.7 V	1.5 V	2.7 V
3.0 V to 3.6 V	1.5 V	2.7 V

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 Data set-up and hold times for the nA_n and nB_n inputs to the nLE_{AB} , nLE_{BA} , nCP_{AB} and nCP_{BA} inputs.

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TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

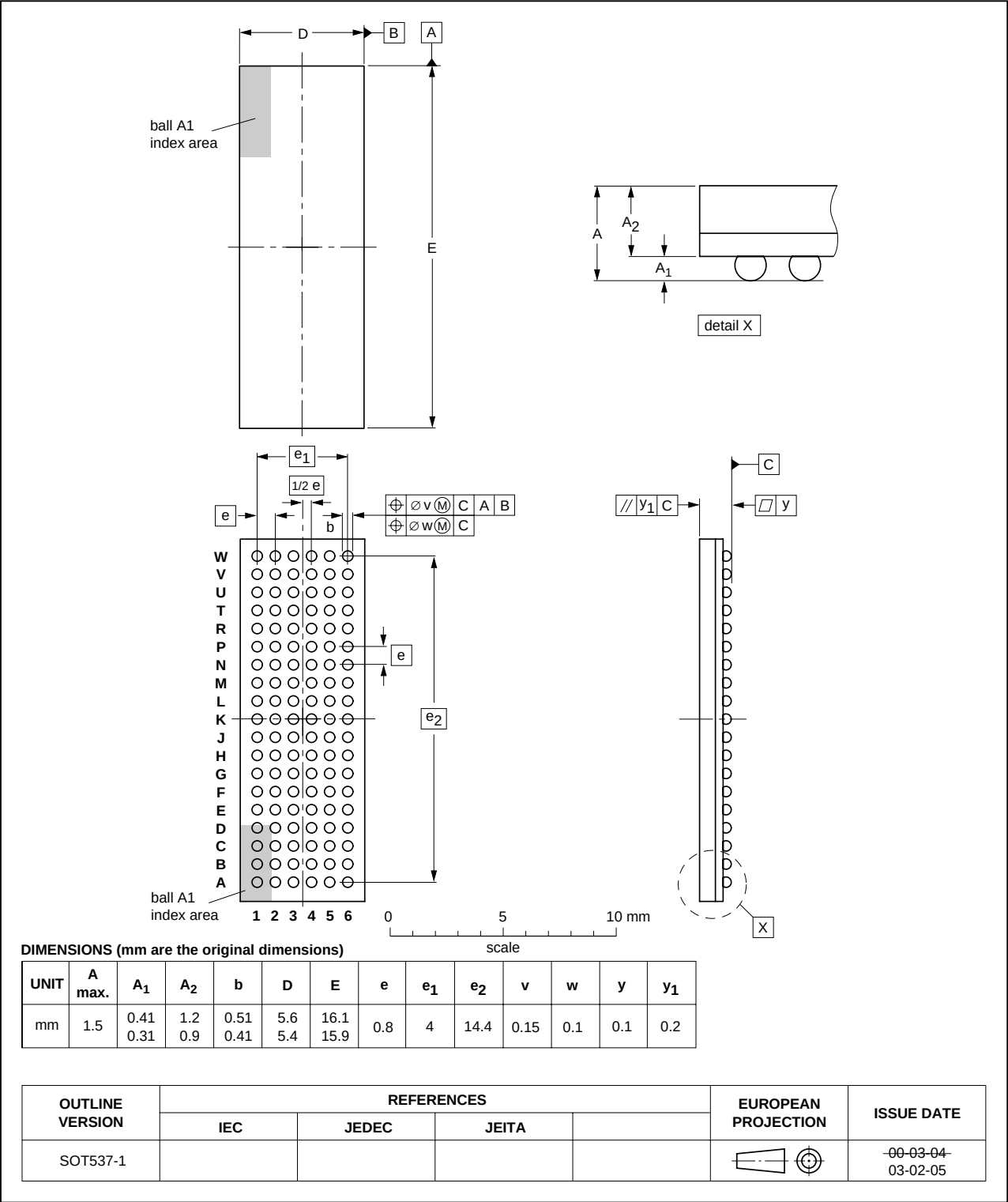
Fig.8 Load circuitry for switching times.

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PACKAGE OUTLINE

LFBGA114: plastic low profile fine-pitch ball grid array package; 114 balls; body 16 x 5.5 x 1.05 mm SOT537-1



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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

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